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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet	1	of	2
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Complete if Known

Application Number	101630,615
Filing Date	07/30/2003
First Named Inventor	Josey G. Angilivelil
Art Unit	2825
Examiner Name	NGTHA M. DEAN
Attorney Docket Number	TI-34945

U. S. PATENT DOCUMENTS

[illegible]

FOREIGN PATENT DOCUMENTS

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**Examiner
Signature**

Aughah

Date
Considered

11/28/05

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		Application Number	101630,615
		Filing Date	07/30/2003
		First Named Inventor	Josey G. Angilivelil
		Art Unit	2826
		Examiner Name	NGHIA M. DOAN
Sheet 2	of 2	Attorney Docket Number	TI-34945

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
NMD		SAMY R. MAKAR and EDWARD J. MCCLUSKEY, "Iddq Test Pattern Generation for Scan Chain Latches and Flip-Flops", Center for Reliable Computing Stanford University. (date unknown)	
NMD		SAGAR SBADE and DUNCAN M. WALKER, "Iddq Test: Will It Survive the DSM Challenge", Department of Computer Science Texas A&M University, pp. 1-18, (date Unknown)	
NMD		KRISTIAN WIKLUND, TOMAS MAGNUSSON and PETER DAHLGREN, "Switch-Level Fault Simulation and Test Generation For Competing Bridging Faults", Department of Computer Engineering, Chalmers University of Technology. (date unknown)	
NMP		PETER C. MAXWELL and ROBERT C. AITKEN, "Test Sets and Reject Rates: All Fault Coverages ARE Not Created Equal", IEEE Design & Test of Computers, pp. 42-51, March 1993	
NMD		SHARAD C. SETH and VISHWANI D. AGRAWAL, "Characterizing the LSI Yield Equation from Wafer Test Data", IEEE Transactions on Computer-Aided Design, Vol. CAD-3, No. 2, pp. 123-126, April 1984	

Examiner Signature		Date Considered	11/28/01
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